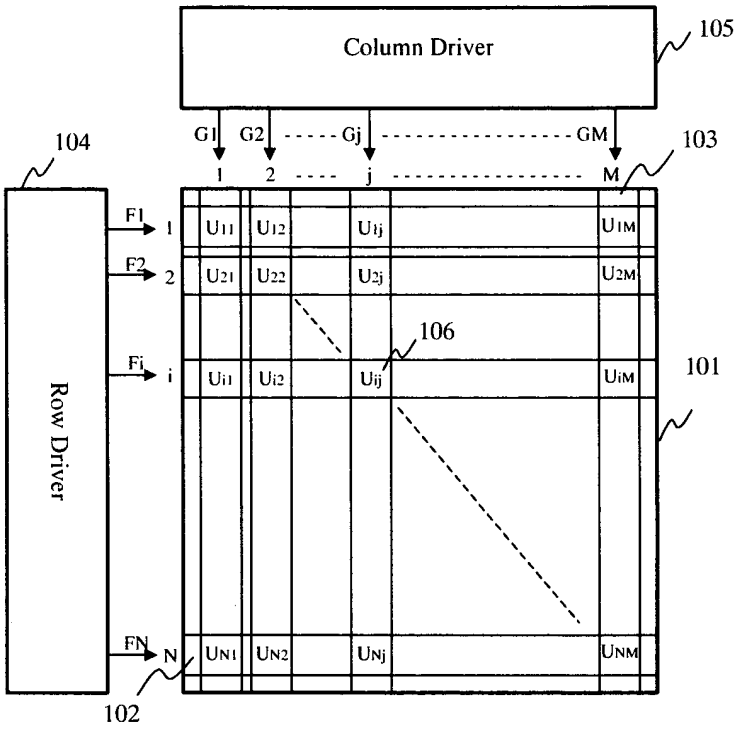

FIG. 1 (Related Art)

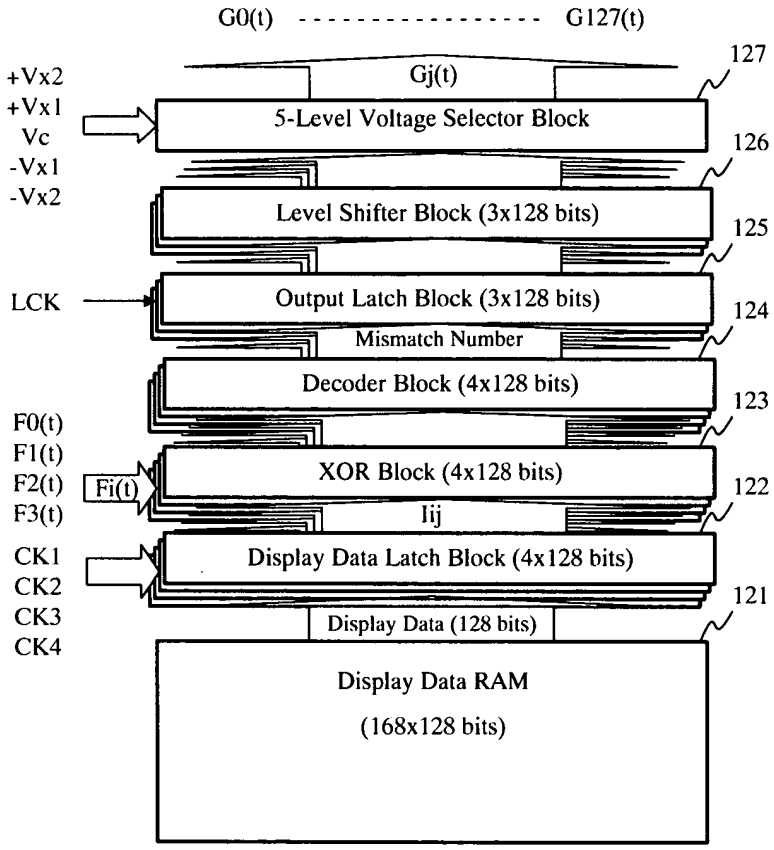

FIG.2 (Related Art)

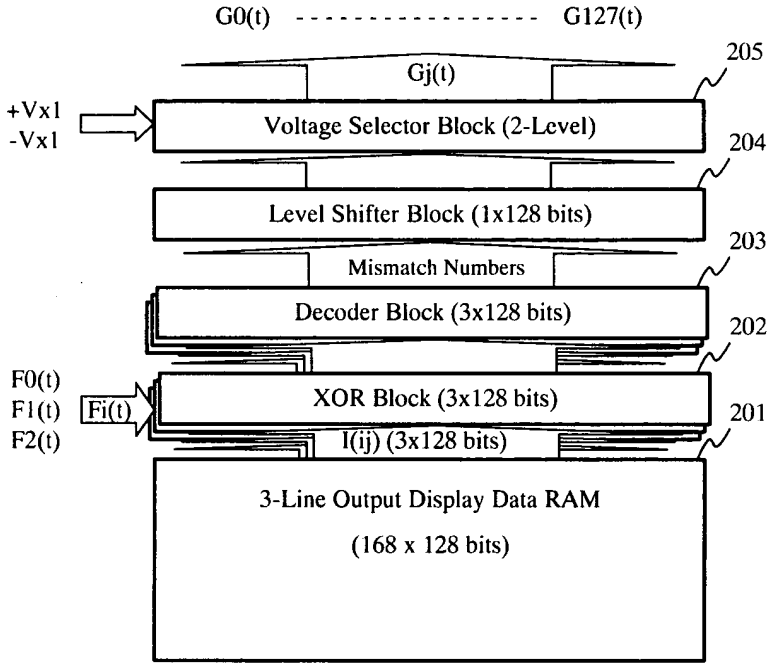

FIG. 3 (Present Invention)

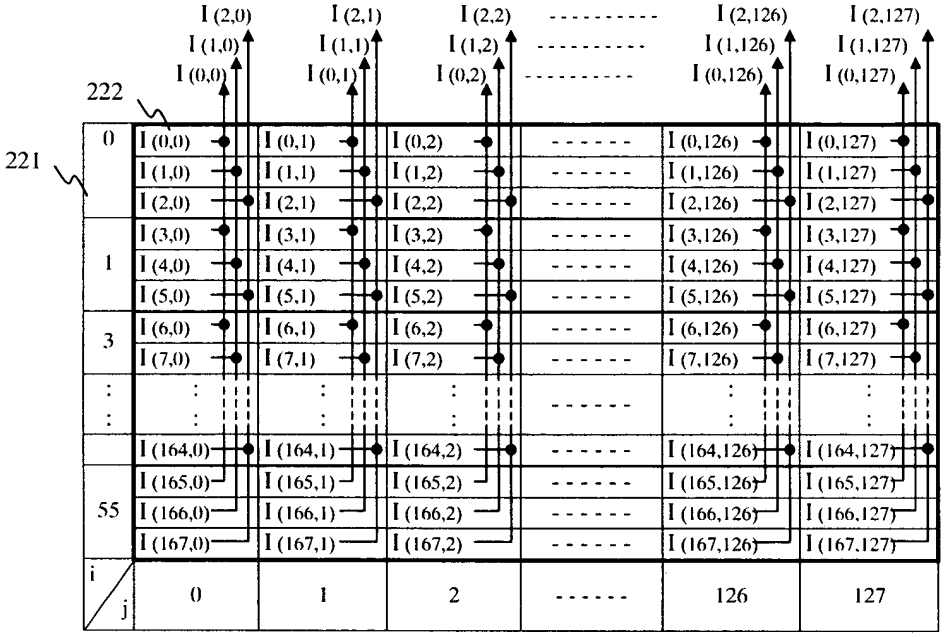
222
221
I (2,0)
I (1,0)
I (0,0)
I (2,1)
I (1,1)
I (0,1)
I (2,2)
I (1,2)
I (0,2)
I (2,126)
I (1,126)
I (0,126)
I (2,127)
I (1,127)
I (0,127)
0
1
3
55
i
j
0
1
2
126
127

FIG. 4

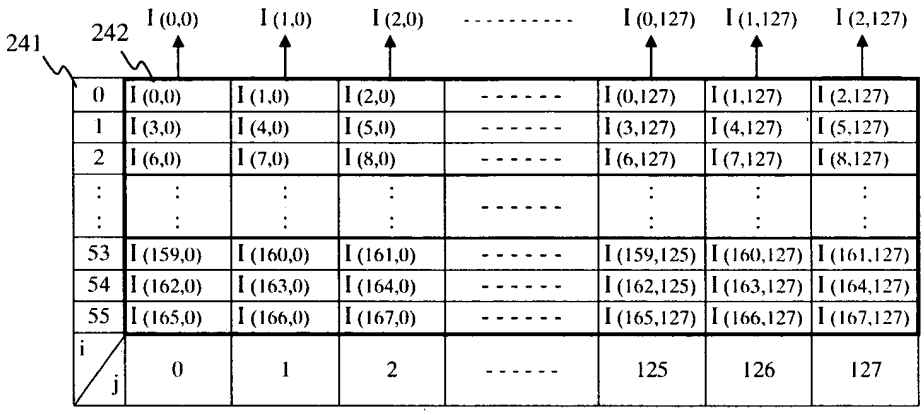
241
242
I (0,0)
I (1,0)
I (2,0)
I (0,127)
I (1,127)
I (2,127)
0
1
2
53
54
55
i
j
0
1
2
125
126
127

FIG. 5

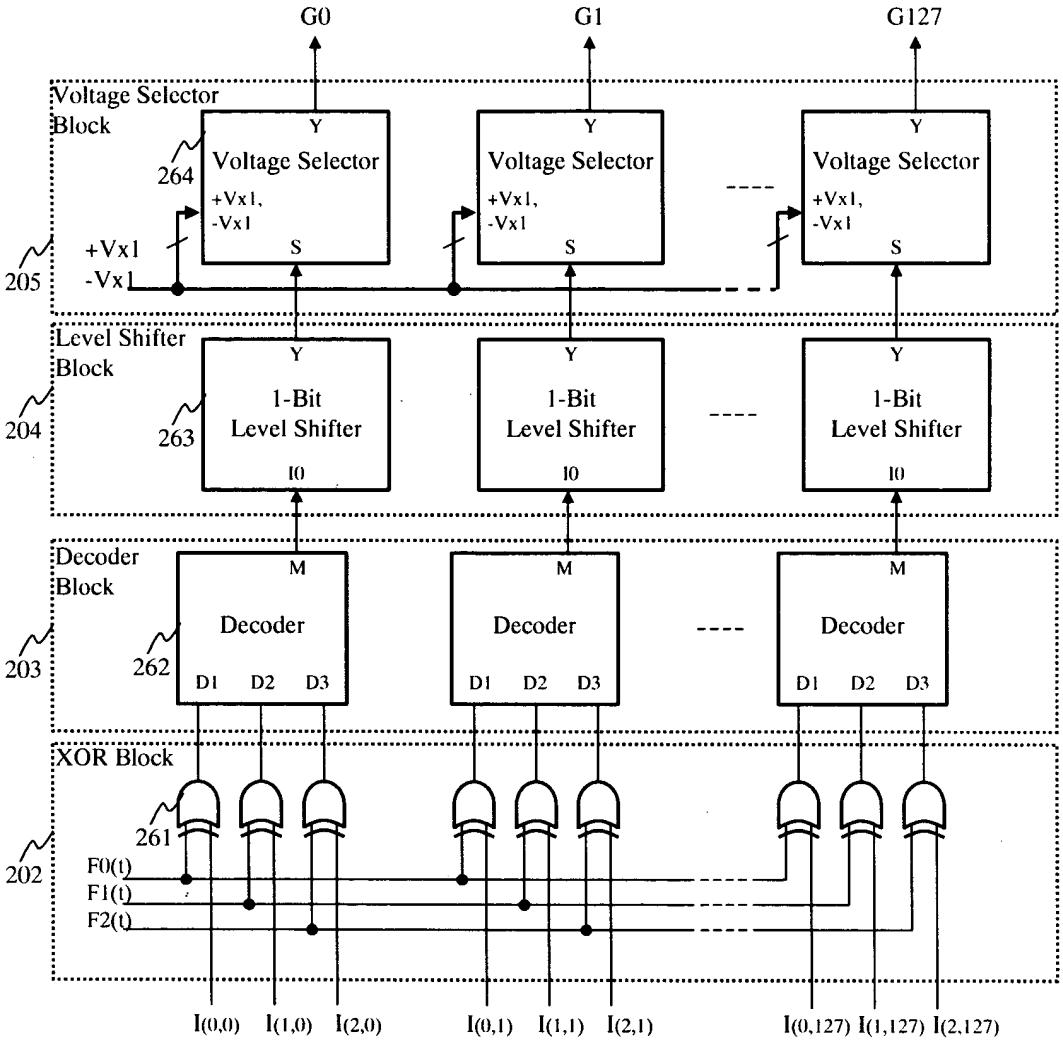
G0
G1
G127
Voltage Selector Block
264
Voltage Selector
+Vx1,
-Vx1
Y
S
+Vx1
-Vx1
205
Level Shifter Block
204
263
1-Bit Level Shifter
I0
Decoder Block
203
262
Decoder
M
D1
D2
D3
XOR Block
202
261
F0(t)
F1(t)
F2(t)
I(0,0)
I(1,0)
I(2,0)
I(0,1)
I(1,1)
I(2,1)
I(0,127)
I(1,127)
I(2,127)

FIG. 6

t / i	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
1	1	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0
2	·	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0
3	1	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
v1	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	:	*0*	*0*	*0*	*0*	*0*	*0*	*0*
4	0	·	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	1	0	0	0	0	0	0
5	0	·	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	·	0	0	0	0	0	0
6	0	·	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
v2	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	:	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*
7	0	0	·	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	·	0	0	0	0	0
	0	0	1	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	·	0	0	0	0	0
9	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	·	0	0	0	0	0
v3	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	:	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*0*
10	0	0	0	·	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	:	0	0	0	0	0	0	0	1	0	0	0	0
11	0	0	0	·	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	·	0	0	0	0
12	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	:	0	0	0	0	0	0	0	1	0	0	0	0
v4	*0*	*0*	*0*	:	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*0*	*0*
13	0	0	0	0	1	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	:	0	0	0	0	0	0	0	·	0	0	0
14	0	0	0	0	·	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	·	0	0	0
15	0	0	0	0	1	0	0	0	0	0	0	0	:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0
v5	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	:	*0*	*0*	*0*
16	0	0	0	0	0	·	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	1	0	0
17	0	0	0	0	0	·	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	·	0	0
18	0	0	0	0	0	·	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0
v6	*0*	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	:	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*0*	*0*
19	0	0	0	0	0	0	·	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	·	0
20	0	0	0	0	0	0	1	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	:	0	0	0	0	0	0	0	·	0
21	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	·	0
v7	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	:	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*0*
22	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	·
23	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	·
24	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	·	0	0	0	0	0	0	0	1
v8	*0*	*0*	*0*	*0*	*0*	*0*	*0*	:	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	:

FIG. 7

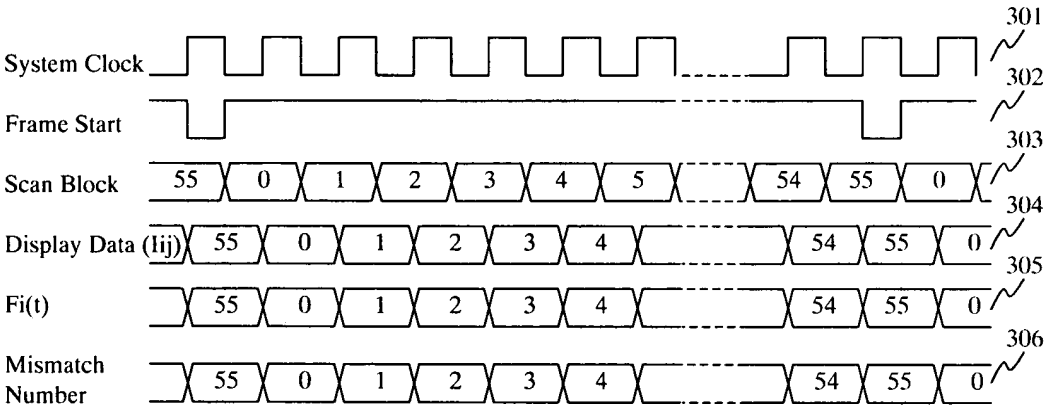
301
System Clock
302
Frame Start
303
Scan Block
55 0 1 2 3 4 5 54 55 0
304
Display Data (Iij)
55 0 1 2 3 4 54 55 0
305
Fi(t)
55 0 1 2 3 4 54 55 0
306
Mismatch Number
55 0 1 2 3 4 54 55 0

FIG. 8

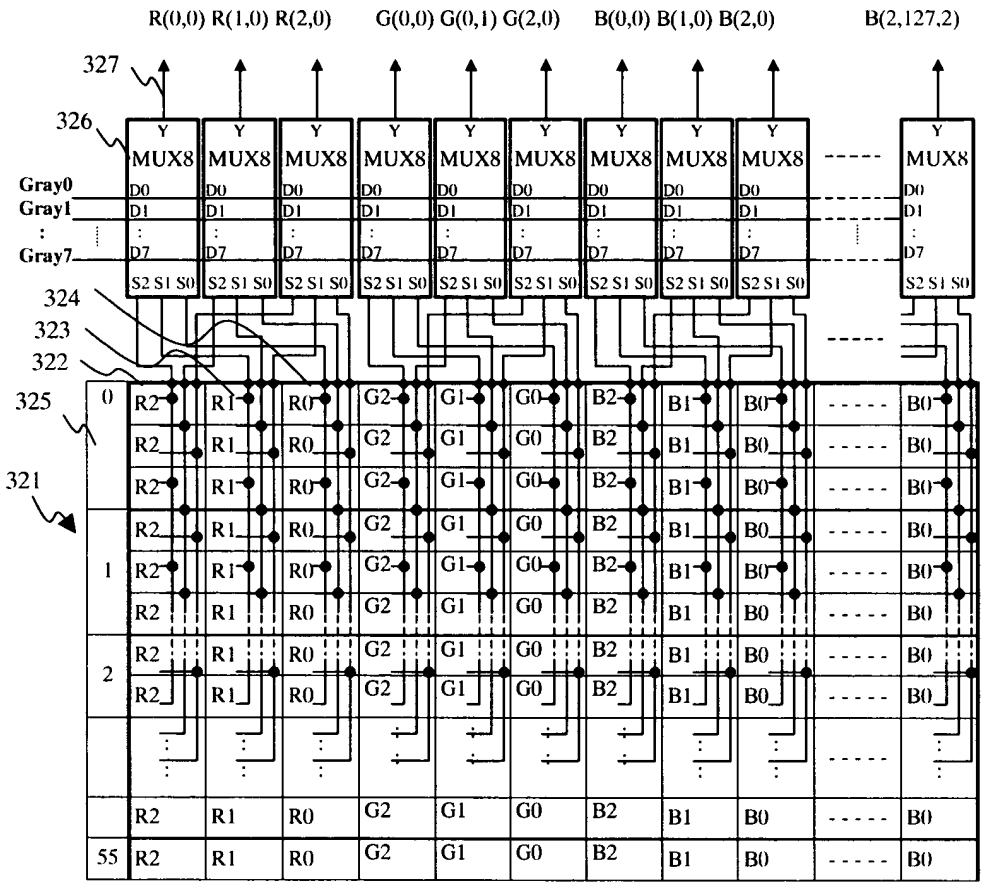
R(0,0) R(1,0) R(2,0) G(0,0) G(0,1) G(2,0) B(0,0) B(1,0) B(2,0) B(2,127,2)
327
326
MUX8
Gray0
Gray1
Gray7
D0
D1
D7
S2 S1 S0
324
323
322
325
321
0
1
2
55
R2 R1 R0 G2 G1 G0 B2 B1 B0

FIG. 9